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Mark Peting

Expertise

High-speed ASIC design, standard cell, and FPGA design. High-speed PCB design and layout, signal integrity, PLL, DLL, CDR. Digital communications: satellite, cable, fiber, & terrestrial. A/D & D/A design, DSP algorithms and implementation, RF design, and photonics. FEC, ECC, cryptography and networking protocols. C, assembly, RTOS, UNIX networking and administration and security.

Experience

2001-Present Chromadyne Beaverton, OR

Founder & CTO

Responsible for system architecture and product design of the following:

- 25 Gsps, 6-bit 4-channel A/D converter
- 25 Gsps, 5-bit 2-channel D/A converter
- Advanced optical transmitter and receiver
- PCB design of 1.5 GHz ECL with sub picosecond timing control
- Advanced fiber communications framer architecture
- DSP algorithms for ultra-long haul fiber telecommunications systems

1998-2001 Geocast Network Systems Beaverton, OR

Founder & Hardware Systems Architect

Responsible for product definition and system architecture for the following:

- Single-chip whole satellite (1Gb/s) demodulator using novel DSP algorithms to minimize silicon area
- Advanced, low-cost, MIPS-based home server
- High-performance MIPS system controller with cryptography engine
- ATSC playback and record system for analysis of digital, terrestrial reception

1997–1998 PMC-Sierra Beaverton, OR

Architect

Responsible for chip-level macro and micro architectures as well block-level implementation.

- Responsible for the architecture the PM3390, an 8 Gb/s switching fabric. The design was developed in .35 *u*m CMOS technology and comprised 400,000+ gates and nearly 245,000 bits of storage.
- Responsible for the gate-level implementation and verification of a hardware linked list manager that was the central intelligence for the switch fabric.

1997 PMC-Sierra Beaverton, OR

Senior Product Design Engineer

Member of the team responsible for developing the PM3351, an 8-port, 10BASET Ethernet switch chip.

- Using Verilog, developed the test suites used to verify the MAC interface, and the suites used for system-level confidence testing.
- Responsible for a board level / FPGA prototype for a 100 Mb/s Ethernet switch chip.

1994–1997 PMR (acquired by Pointshare) Beaverton, OR

Founder & Architect

Lead architect and designer for database system to link all medical facilities within Oregon.

- Responsible for the communication protocol design and implementation and for the larger wide area network design and implementation
- Developed large database, translator software and developed the middleware.
- Evaluated vendors and made the software vender selection.

1989–1994 Peregrin Technologies Beaverton, OR

Founder & Architect

Lead architect and designer for point of sale terminals.

- Responsible for the architecture and design of both the hardware and software for POS terminals.
- Developed the security modules and financial transaction protocols software.
- Developed an RTOS and integrated ethernet and TCP/IP protocol software into the system.
- Responsible for the design of electromechanical control hardware and the modem hardware.

1986–1989 Hardware Design Consultant Oregon & California

Hardware Design Consultant

As an independent design consultant, designed and implemented a number of hardware and software projects.

- POS hardware, RTOS, a video display ASIC, a rendering engine, and measuring instrumentation.

1982–1986 Eltronix Coos Bay, Oregon

Architect & Founder

Responsible for the architecture and implementation of both hardware and software

for a multiprocessor personal computer.

- Developed architecture for a multiprocessor system with cache coherence on multiple memory buses.
- Designed a RS based ECC memory.
- Developed a novel video display system and a mass storage system
- Designed and implemented a novel 300mbs LAN hardware and protocol system.

Patents

US20020056100, US20020009135, US5918720

Education

1983-1987 California Institute of Technology Pasadena, CA
B.S. Electrical Engineering