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Jim Jackson

Expertise

Executive and Project level management. High-speed ASIC design, validation, & verification. FPGA design. C/C++ and UNIX device driver development. Multiprocessor design, ECC, and networking protocols.

Experience

2002-Present High Speed Circuit Consultants Portland, OR

Managing Partner

Started a four-person consulting firm focused on the development of high performance digital and analog systems.

- Developed an Altera-based FPGA and testbench that resolved trigger times to within 2 ps for a high performance analog VLSI tester.
- Developed the characterization and calibration software (in C) for the aforementioned trigger measurement system.
- Helped develop a web-based expert system based on mySQL as an aid for those who wish to quit smoking.

2001-2002 Chromadyne Beaverton, OR

Founder, General Manager & VP Engineering

Started a 12-person design center responsible for the development of a technology prototype for a high-performance long-haul transmission system.

- Raised $4.5M in venture funding to develop hardware prototype.
- Responsible for many levels of management within the company: developed budgets, schedules, funding presentations, and ran day-to-day design.
- As an individual contributor, developed LINUX drivers for high-speed data acquisition and control system and developed a number of low-level SW applications for the prototype system.

1999-2001 Geocast Network Systems Beaverton, OR

VP HW Engineering

Led 40-person design group responsible for the development of the Geocast Personal Server, a caching system that could receive content via digital terrestrial, cable, or satellite broadcast.

- Responsible for an $8.5M annual budget.
- Ran group with three independent ASIC design teams, custom IC design team, PCB development, and manufacturing interface teams.
- Worked with key manufacturing and distribution partners like Thomson Consumer Electronics / RCA to promote and manufacturer a new piece of consumer electronics.
- Worked with TSMC and Amkor to develop IC fabrication relationships.

1998-1999 Geocast Network Systems Beaverton, OR

Director HW Engineering

Started HW Design Center, and built the team to 25 before being promoted.

- Led team that developed a 125 MHz MIPS system controller with custom encryption engine and dual IDE / PCI interfaces that was the centerpiece for the Geocast Personal Server. This chip was developed using 0.35*um* technology and was comprised of 500,000+ gates. Additionally, developed the guided pseudo random testbench for verifying this chip which was a first pass success.
- Developed technology roadmap and hiring plan and was personally responsible for hiring the initial 25 ASIC, custom design, and PCB engineers.

1997–1998 PMC-Sierra Beaverton, OR

Project Leader

Led six-person design team responsible for creating the PM3390, an 8 Gb/s switching fabric. The design was developed in .35 *u*m CMOS technology and comprised 400,000+ gates and nearly 245,000 bits of storage.

- Responsible for defining the chip architecture, design specification, and scheduling, as well as creating the chip testbench, developing and executing the verification plan, and taking the design through synthesis, place and route, test-vector creation, and production test.
- Responsible for recruiting and building the design team at PMC. This included hiring four members of the PM3390 design team and several other members of the hardware and firmware groups.
- Responsible for evaluating the performance of all members of the hardware design group and for writing performance evaluations for the PM3390 team.

1997 PMC-Sierra Beaverton, OR

Senior Product Design Engineer

Member of the team responsible for developing the PM3351, an 8-port, 10BASET Ethernet switch chip.

- Implemented the transmit and receive logic for the MAC interface of the PM3351.
- Using Verilog, developed the test suites used to verify the MAC interface, and the suites used for system-level confidence testing.

1994–1997 Pyramid Technologies Beaverton, OR

Senior Member of Technical Staff

Led the effort to create and implement the chip-level and system-level validation environment for a major computer system.

- Developed the design verification strategy and implemented ASIC testbenches using Verilog for two 200,000+ gates LSI 500K designs. This included interfaces to the MIPS R10000 Avalanche bus, the PCI bus, and a

proprietary MPP switching fabric.

- Helped develop a multi-dimensional MPP fabric analysis simulator used to determine what connectivity scheme would be used for a massively parallel computer system.

1991–1994 Convex Computer Richardson, TX

Software Project Leader

Developed and led a five-member team responsible for creating the Convex Expert Troubleshooting System (CXTS). Was responsible for architecting the system, developing project plans and schedules, and implementing the system using C++.

- Using C++, developed a completely user-configurable rules database and troubleshooting system that reduced maintenance overhead and increased system availability.
- Developed an X-Motif GUI for the entire system using Xdesigner.
- Created an interface to the corporate-quality database that allowed real-time data from all field sites to be automatically logged and analyzed.

1989–1991 Convex Computer Richardson, TX

Hardware Design Engineer

Member of the two-person design team that developed the MCM3, the memory subsystem used in the Convex C2, C3200, and C3400 supercomputers.

- Designed an 8,000-gate CMOS array that implemented the control logic for interfacing to dynamic RAMs on the board. Responsibilities included the behavioral modeling, gate implementation, synthesis, and test vector generation for the array.
- Was issued U.S. Patent #5,291,498 for the Error Correcting Code that I developed and implemented in the array.
- In 3/90, became the lead engineer and was responsible for the placement, routing, board-level simulation, and timing verification of the entire subsystem.

Education

1987-1988 University of Illinois Urbana, IL

- M.S. Electrical Engineering 4.8/5.0
- M.S. Thesis: Developed a behavioral model for an ECL gate array that implemented the protocol for the IEEE Standard for Fastbus, a high-speed data acquisition and control system.
- Specialized in Computer Architecture.

1983-1987 University of Illinois Urbana, IL

- B.S. Electrical Engineering 4.2/5.0