8152 SW Hall Blvd PMB #120
Beaverton, OR 97008
(503) 567-9016 (work)
daleb@.hscc.biz

Dale Beyer

Expertise

High-speed ASIC design, validation, & verification. FPGA design. DSP algorithms, C, photonics, multiprocessor design, cache coherency, and PCI.

Experience

2001-Present Chromadyne Beaverton, OR

Project Leader

Led group responsible for the development of DSP algorithms used to mitigate the effects of linear and non-linear effects for a fiber optic transmission system.

- Investigation of Linear and Non-Linear effects in optical fiber.
- Developed a model of four-wave mixing in optical fiber.
- Characterized components in a optical fiber system.
- Developed Verilog for FPGA in an optical control loop.

1999-2001 Geocast Network Systems Beaverton, OR

Senior Design Engineer

Responsible for ATPG methodology and DSP development.

- Responsible for debug of ATSC playback and record system.
- Conducted research into ATSC reception quality and ghosting and developed software to measure and display realtime echos seen in recorded data.
- ATPG Methodology development for chip design flow, generated vectors for 3 chips.
- Used Chrysalis on custom cells to verify ATPG model is same as implemented version
- Responsible for the design of the Symbol loop development on a large satellite demodulator. Converted floating point model to fixed point version.

1997-1999 Sequent Beaverton, OR

Intermediate System Engineer

Developed ASIC and board level logic for the StiNG II.

- ASIC designer of IO section on ~1 million gate design.
- Tested and debugged basic functionality problems.
- Lead debug engineer in lab for early silicon validation of next generation baseboard STiNG II.
- Assumed Technical Project lead for baseboard of STiNG II.
- Used perl to design Verilog coding and baseboard routing tools.
- Knowledgeable in PCI, and several Intel proprietary buses.

1996 Sequent Beaverton, OR

Intern

- Worked on the validation team of STiNG, Sequent's NUMA-Q Pentium Pro systems
- Performed subsystem validation of the Pentium Pro baseboard
- Wrote a PCI Bus analyzer for the Tek DAS 9200
- Root cause failure analysis on problems with PCI cards
- Aided in the debug of engineering machines in the company

1995 Intel Hillsboro, OR

Intern

- Worked in the motherboard design division, OMCO
- Designed a PCI Card interface for Flash Memory, applied for patent
- Debugged and evaluated Motherboards
- Learned and used Cadence, Sig Noise, SPEED, and Altera's Max Plus Software

1994 Planar Systems Beaverton, OR

Intern

- Worked on a 16 level Gray scale Display for R&D
- Aided in debugging circuitry and making design changes
- Used Pspice to simulate circuit changes
- Designed interface to download new gray scale parameters to display
- Learned and used Orcad, Visual Basic, & Workview (Xilinx code)

Education

1996-1997 Oregon State University Corvallis, OR

- M.S. Electrical Engineering & Computer Engineering
- M.S. Thesis: Memory optimization for a parallel Sorting Hardware Architecture
- Specialized in Computer Architecture.

1992-1996 Oregon State University Corvallis, OR

- B.S. Computer Engineering Summa Cum Laude. GPA 3.94/4.0